10/643,585

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Please amend the paragraph beginning at line ~~30~~ 29, page 2, as follows:

Figure 1shows one embodiment of an MSP 100. The MSP 100 includes two processors ~~110~~ 900 and two cache memories 120.

Please amend the paragraph beginning at line 11, page 3, as follows:

Figure 9 shows one embodiment of processor ~~110~~ 900. Each processor 110 is composed of a scalar processor 910 and two vector pipes 930. The scalar and vector unit are decoupled with respect to instruction execution and memory accesses. Decoupling with respect to instruction execution means the scalar unit can run ahead of the vector unit to resolve control flow issues and execute address arithmetic. Decoupling with respect to memory accesses means both scalar and vector loads are issued as soon as possible after instruction dispatch. Instructions that depend upon load values are dispatched to queues where they await the arrival of the load data. Store addresses are computed early and their addresses saved for later use. Each scalar processor 910 is capable of decoding and dispatching one vector instruction (and accompanying scalar operand) per cycle. Instructions are sent in order to the vector units, and any necessary scalar operands are sent later after the vector instructions have flowed through the scalar unit's integer or floating point pipeline and read the specified registers. Vector instructions are not sent speculatively; that is, the flow control and any previous trap conditions are resolved before sending the instructions to the vector unit. For a further description of decoupled vector architecture please refer to the U.S. patent application entitled "Decoupled Vector Architecture", filed on even date herewith, the description of which is hereby incorporated by reference.

Please amend the paragraph beginning at line 28, page 3, as follows:

In another embodiment, processor ~~110~~ 900 contains a cache memory 920 for scalar references only. Local MSP cache coherence is maintained by requiring all data in processor cache memory 920 to be contained in MSP cache memory 120.